



Submission Guidelines

Call for Design Platform

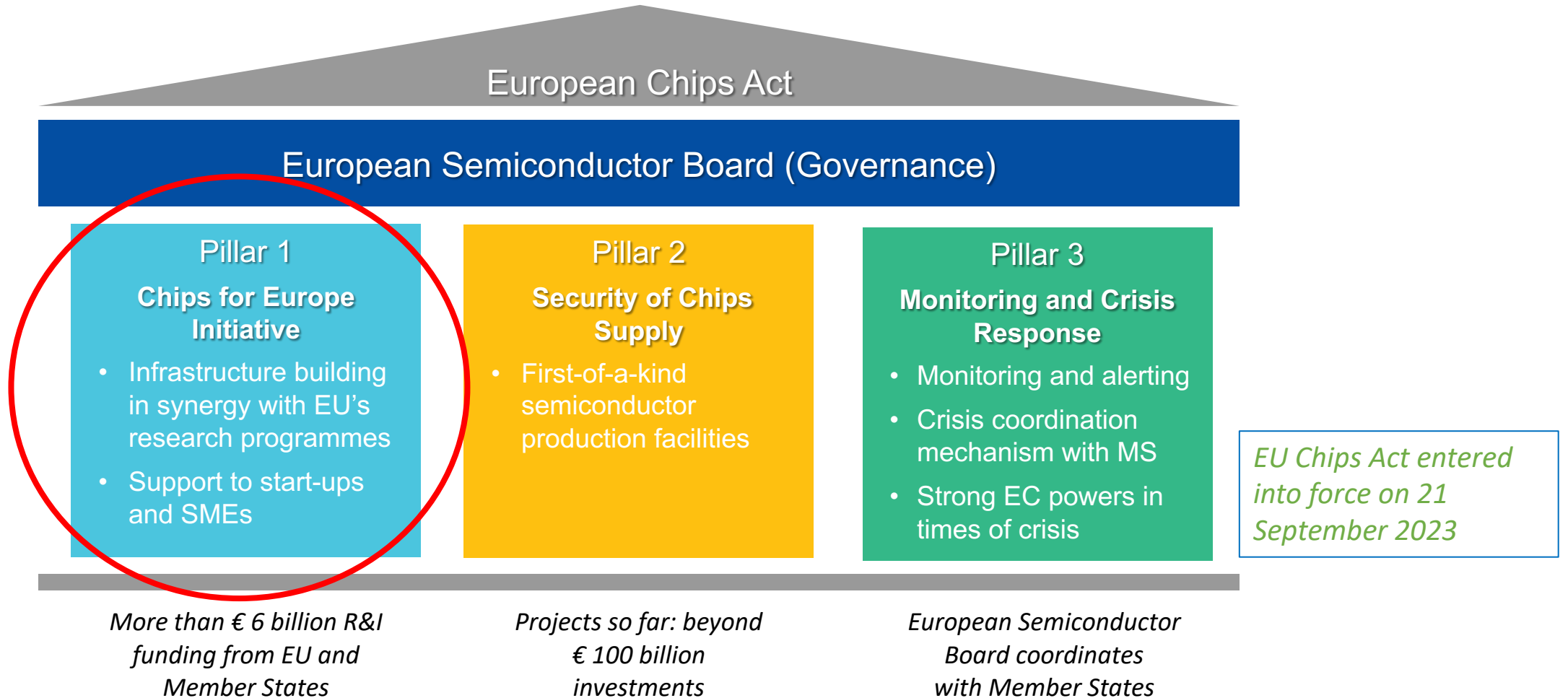
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11/07/2024

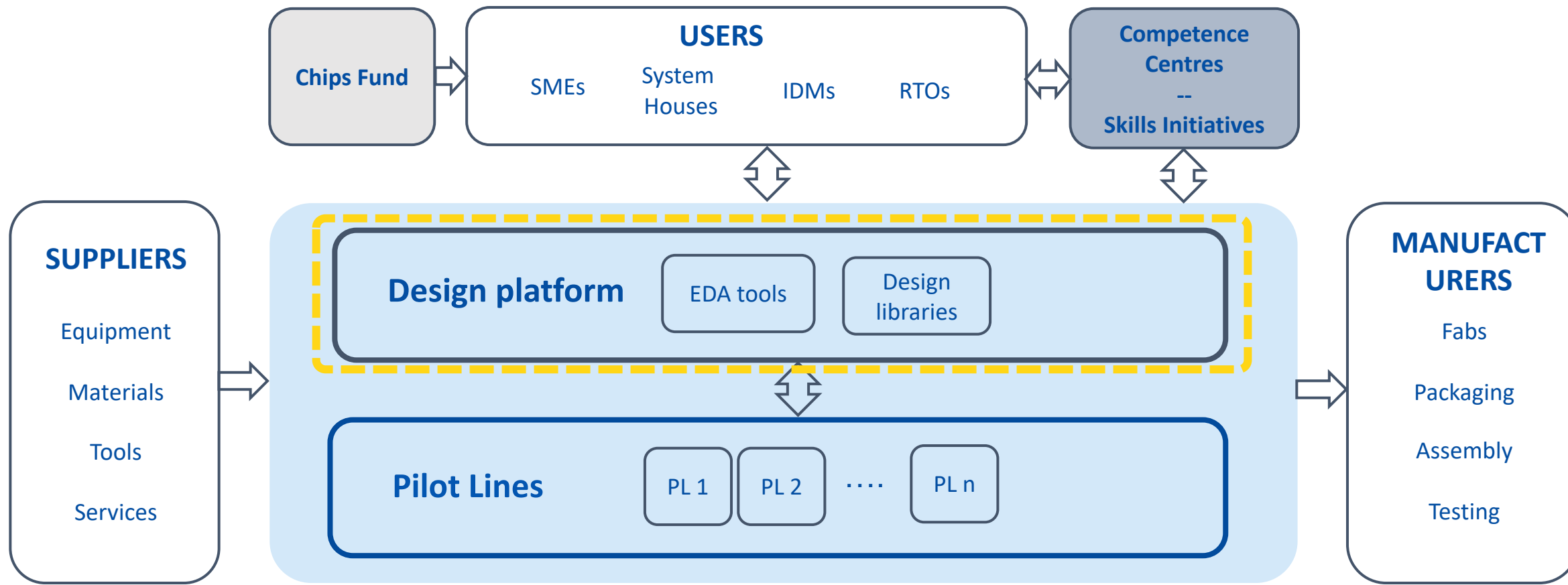
EUROPEAN
PARTNERSHIP



THE EU CHIPS ACT



Chips for Europe Initiative



Call for Design Platform Publication

Chips-2024-CDP-1: Call for Design Platform

EU Expenditure
Max. 25 Mio EURO

Chips for Europe Initiative Calls

Addressing key objectives such as boosting technological sovereignty, ensuring supply chain resilience, & positioning Europe as a leader in advanced semiconductor technologies.

Open Competence Centres Chips-2024-CCC-1 Click here →	Open Support to the European Network of Chips Competence Centres Chips-2024-CCC-2 Click here →	Coming Soon Pilot Line on Advanced Photonic Integrated Circuits Chips 2023-CPL-5 Click here →	Coming Soon Design platform Chips-2024-CDP-1 Click here →
Closed Pilot line on Advanced sub 2nm leading-edge system on chip technology Chips 2023-CPL-1 Click here →	Closed Pilot line on Advanced Fully Depleted Silicon On Insulator technologies targeting 7nm Chips 2023-CPL-2 Click here →	Closed Pilot line on Advanced Packaging and Heterogenous Integration Chips 2023-CPL-3 Click here →	Closed Pilot line on Advanced semiconductor devices based on Wide Bandgap materials Chips 2023-CPL-4 Click here →

<https://www.chips-ju.europa.eu/callsinfo/>

Publication Date: 4 July 2024

Call Opens: 13 August 2024

**Call Closes: 10 October 2024
(17:00:00 GMT+1)**

Call Text Chips-2024-CDP-1

Location:

Appendix 4 of the **Chips JU Multi Annual Work Programme (MAWP)** -
<https://www.chips-ju.europa.eu/CDP-1/>

(Sub)sections concerning the Call for Design Platform:

- **Subsection 2.4.** Chips-2024-CDP-1: Design platform
- **Section 4.** DESCRIPTION OF THE CALL FOR DESIGN PLATFORM (CDP)

Context of Chips-2024-CDP-1 – Call for Design Platform (Appendix 4 of the Chips JU WP)

- Semiconductor circuit **design** constitutes a **substantial portion of the added value** within the chips value chain.
- The trend is moving towards more **complex, application-specific, highly integrated** semiconductors.
- **Pillar I** of the Chips Act, outlines an ambitious plan for promoting the **growth of fabless companies** focused on **leading-edge technologies**.
- This activity aims at building a pioneering cloud-enabled **European Design Platform (DP)** that will aid users to develop chips.
- The main **target users** of the DP shall be **commercial entities**, particularly **start-ups** and **SMEs**, for the purpose of **pre-competitive activities** such as research, development and innovation up to experimentation and tape-out.
- This call concerns the selection of the consortium in charge of the overall coordination of the Design Platform, referred to as the **Platform Coordination Team (PCT)**, which shall serve as the **hosting entity** of the central cloud infrastructure.
- The **PCT shall:**
 - **operate** the overall DP initiative and will **manage** the developments of its users.
 - **assist the Chips JU** in defining the **technical specifications** of the cloud service for the platform to be **procured by the Chips JU** through a dedicated *Call for Tenders* for the procurement of the cloud service
 - be responsible for coordinating training, EDA tool and IP licensing support and the coordination of decentralised teams referred to as **Design Enablement Teams (DETs)**.
- The Design Platform shall complement the ongoing EUROPRACTICE initiative. It is anticipated that in the future EUROPRACTICE's services may be integrated into the Design Platform

Expected Outcomes of Chips-2024-CDP-1 – Call for Design Platform (Appendix 4 of the Chips JU WP)

- Easy **cloud-enabled access to EDA** tools (including **proprietary** and **open-source** tools), libraries of design templates, training and support services.
- The cloud services may be developed and maintained by third parties, however the **PCT**, in line with a **Hosting Agreement**, shall assume **responsibility for the coordination and execution** of the various related activities.
- The PCT shall oversee that the **cloud service** is **secure, scalable, and accessible 24/7**. The service shall include the provision of a **user help desk support**, robust **security** measures, **data backup and recovery**, and regular **maintenance and updates**.
- The PCT shall **continuously monitor the operation** of the Design Platform and the **quality of services** provided to users. This includes incorporating **user feedback** loops and adopting corrective measures as necessary.
- The **management and maintenance** of a **cloud-based repository** for the European chip design community, populated with an extensive portfolio of open-source and proprietary 'design assets' to facilitate and enhance the design process for users.
- A **quicker and more efficient licensing process** for commercial EDA tools and IP libraries, reducing burden and barriers for companies engaging in chip design, coupled with a start-up support programme, that includes financing of licensing costs.
- **Integration** in the Design Platform of the **design support services** provided by specialised design service providers, known as **Design Enablement Teams**, that will be designated following a **subsequent linked call**.
- Advanced **training and support services** available to a wide range of users via the Design Platform complementing the the network of Competence Centres or potential future dedicated actions across the Union.

Scope of Chips-2024-CDP-1 – Call for Design Platform (Appendix 4 of the Chips JU WP)

- The purpose of this call is to select a consortium that will be responsible for implementing, hosting and running the Design Platform and coordinating its development, operation, and maintenance. Activities to address:
 1. **Comprehensive Planning and Development** – define development and implementation targets, milestones, and key performance indicators (KPIs); establish advisory groups to provide critical insights and guidance
 2. **Cloud service management** - provide *technical specifications* for the procurement of the cloud services; *validate, test, manage and maintain* the cloud service; establish and maintain a *repository* of intellectual property (IP), EDA tools, and other design assets.
 3. **Complementarity to other objectives of the Chips for Europe Initiative** - integrate PDKs/ADKs and services stemming from the *pilot lines* into the DP; work closely with *Competence Centres*; support the design development of *quantum chips* withing Chips JU activities; organise and provide advanced *training programmes* for users and developers.
 4. **Technical Requirements and Standards** – outline and provide the *technical requirements, specifications, and service quality standards* necessary for the selection and integration of the DETs; implement *monitoring procedures* to ensure that the DP and the DETs meet the established *technical standards and performance metrics*; undertake *continuous monitoring* of DP's operations and the *quality of services* it provides.
 5. **Supplier Negotiations and Management** – under the *direction and mandate of the Chips JU*: conduct *negotiations* with key suppliers of EDA tools and IP blocks; establish and manage suitable master *framework agreements* with them.
 6. **Start-up and SME support** – provide *technical and operational support* to the Chips JU in the execution of *calls for proposals* from eligible fabless companies; ensure the provision of a dedicated *24/7 user help desk* support to assist the operation of the Design Platform; run a *start-up incubation and acceleration* programme as set out in **Annex C** in Appendix 4 of the Chips JU WP.
 7. **Dissemination and User Engagement** - effectively disseminate to *potential users* the services offered via the Design Platform.

Chips-2024-CDP-1: Two Interrelated Calls

DIGITAL-Chips-2024-CfEol -CDP-1

Call for Expression of Interest (CfEol)
for the selection of a
Hosting Consortium
(no funding)

DIGITAL-Chips-2024-CSA-CDP-1

**Call for proposals for
coordination of the
Design Platform, CSA**
funded under the
Digital Europe (DEP)
(25 Mio EURO funding)

**100% EU
funding -
up to
25 Mio€**

Appendix 4 of the Work
Programme – Activities
launched in 2024 for the
initiative part

Call documents: templates and guidelines –
organized in CfEol and DEP folders

Both calls close at the same
time - **10 October 2024**
(17:00:00 GMT+1)



MAWP Appendix 4

Click here →



Call Documents

Click here →



Proposal Submission

Click here →

Chips-2024-CDP-1: Focus of the Calls

Chips-2024-CDP-1: Design Platform

Call for Expression of Interest (CfEol)

No funding

- Hosting Consortium
- Commitment to sign a Hosting agreement

The PCT will **host infrastructure & services.**

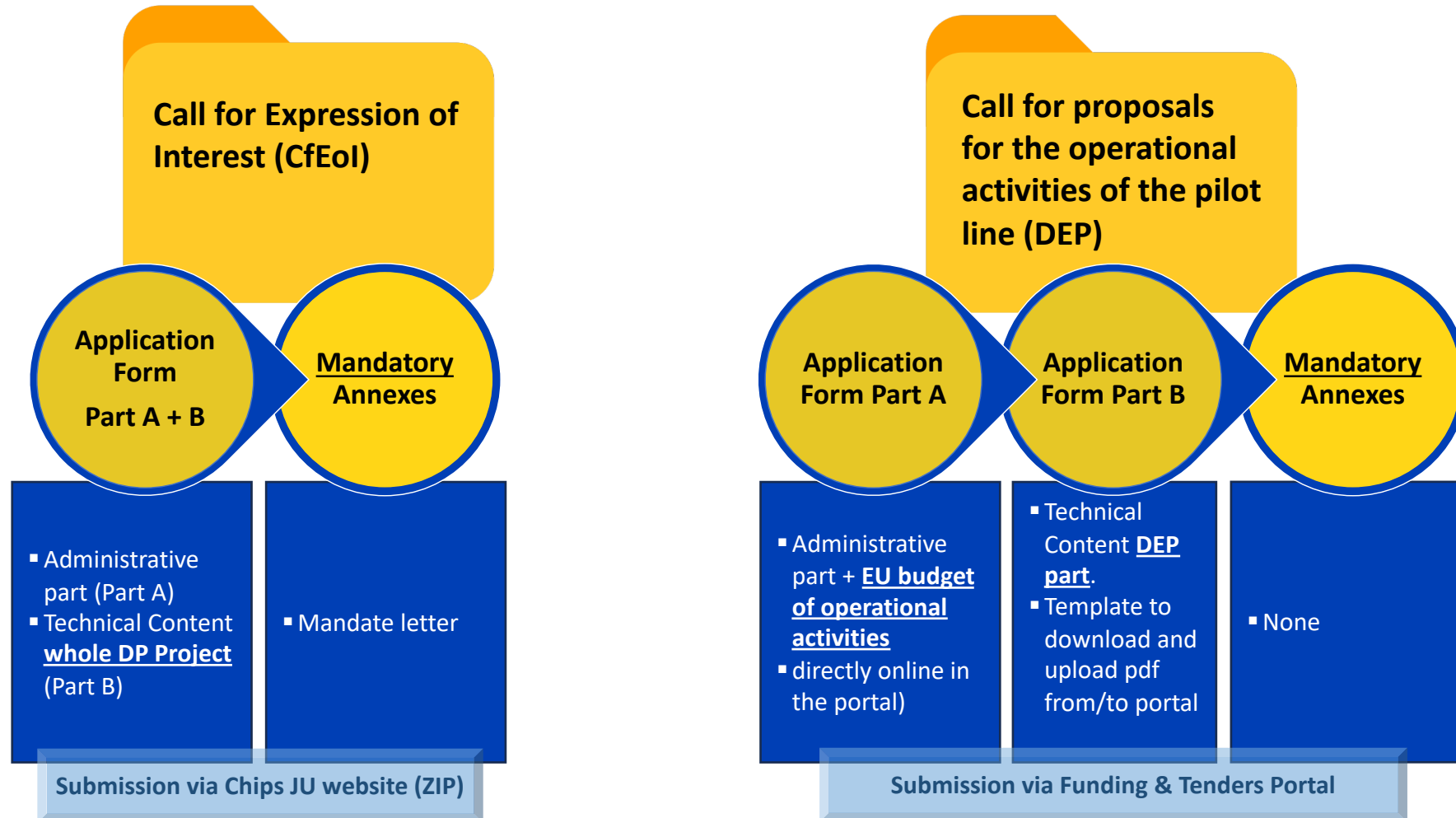
Chips JU will **procure services** following specifications defined by the PCT.

Call for proposals for the for coordination of the Design Platform (DEP)

100% EU funding - up to 25 Mio€

- coordination and operational activities
- standard operating costs of the Design Platform
- Technical support to Chips JU for DP procurements and calls

Chips-2024-CDP-1: Submission Documents



Note: **Part B of the DEP** call shall be **appended** to the **CfEol** application in a **single zip file**.

Eligibility Criteria - CfEol

The call is open to entities or consortia of entities fulfilling **cumulatively the following conditions**:

- a) The **Hosting Consortium** shall include the members that will host and coordinate the Design Platform. Said consortium shall also run the operations of the Platform Coordination Team. The members of the consortium shall be from a **Participating State to the Chips JU**.
- b) A **consortium must consist of**:
 - a) **at least one** independent legal entity **established in a Member State**; and
 - b) **at least two** other independent legal entities each established in a different **Participating State**;
- c) **The members** of the Hosting Consortium shall be **registered** as a legal entity in **one of the Participating States**; The applicant(s) shall have a legal personality on the date of the deadline for submission of applications and must be able to demonstrate their existence as a legal person.

The coordinator must be **given a mandate to represent** the other members of the Hosting Consortium to sign and administrate the **Hosting Agreement** and the various **associated grants**.

Eligibility Criteria – DEP CSA

Eligible participants (eligible countries) - **the applicants** (beneficiaries and affiliated entities) must:

- be **legal entities** (public or private bodies)
- be **established** in one of the **eligible countries**, i.e.:
 - EU Member States (including overseas countries and territories (OCTs))
 - non-EU countries:
 - EEA countries (Norway, Iceland, Liechtenstein)
 - countries associated to the Digital Europe Programme Specific Objective 6 or countries which are in ongoing negotiations for an association agreement and where the agreement enters into force before grant signature.

Beneficiaries and affiliated entities must register in the **Participant Register** — before submitting the proposal — and will have to be **validated** by the Central Validation Service (**REA Validation**).

Access guiding principles

- **Inclusivity**: Access should be made **available to a wide range of users across the Union** as per specific conditions
- **Transparency**: Information regarding the criteria, processes, and terms governing access to the Design Platform shall be clear and transparent to ensure that potential users have a comprehensive understanding of the access framework.
- **Non-Discrimination**: Access shall be granted on a non-discriminatory basis, avoiding preferential treatment of potential users based on their geographic location, affiliation, etc.
- **Proportionality**: Access by EU users, i.e. users established in the Union, should be (at least) directly **proportional to the financial contribution by the Union** to the total costs of those activities;
- Access needs to be provided on **market terms**, or on a cost-plus-reasonable-margin basis for large undertakings, while granting **preferential access or reduced prices for academic institutions, start-ups and SMEs**.
- Access should be granted to **international research and commercial partners**, if this is foreseen in Digital Partnerships and Trade and Technology Councils of the Union as part of its agreement with its international strategic partners
- In case of **excessive demand** for access to an infrastructure, responsible organisations, in this case the **PCT** consortium, need to put in place mechanisms to ensure **fairness, transparency, and equal opportunity** for all interested parties;

EU added value and economic security considerations

- Access to the Design Platform should be based on **fair and non-discriminatory principles** and should be **limited to Participating States of the Chips JU** (EU Member States, EEA countries and those countries that have been associated to Horizon Europe or Digital Europe Strategic Objective 6, under which the design platform is funded).
- For access of users **established in any Participating State** but **controlled from third countries** that are not Participating States of the Chips JU, consortia must take into consideration the following two main criteria:
 - **EU added value**, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.
 - **Economic security** considerations.

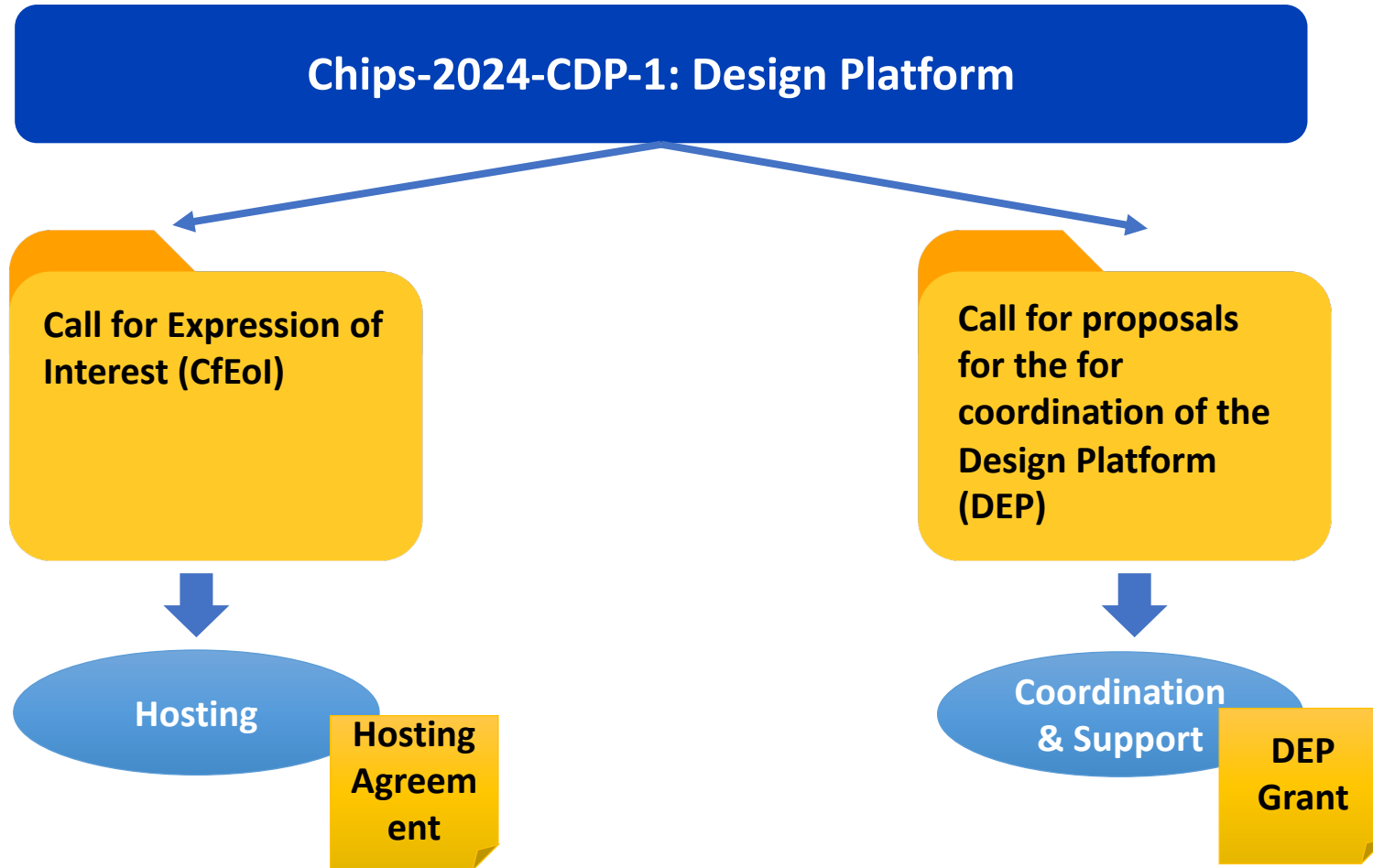
Only users from organisations that can clearly **demonstrate** their **contribution to EU added value** and their alignment with **European economic security** shall be granted access.



Specific Access Provisions

- Regarding **Level 1** services
 - These services should be open to all users in the EU who satisfy some **basic eligibility** criteria to be **proposed by the applying PCT** consortia.
- Regarding **Level 2** services
 - **In addition to** access to Level 2 services via **potential financial support** from the Union and Participating States, companies may get access to these services via **market prices**.
 - Companies could potentially get access to Level 2 services via potential financial support from the Union and Participating States. Any potential competitive funding scheme shall include **EU added value and economic security** considerations as an evaluation criterion.

Chips-2024-CDP-1: Outcomes of the Calls



Only one proposal will be selected for funding.

Chips-2024-CDP-1: Evaluation

Chips-2024-CDP-1: Design Platform

Call for Expression of Interest (CfEol)

Call for proposals for the for coordination of the Design Platform (DEP)

Criterion	Max Score	Threshold
Excellence & Relevance	30	15
Impact	30	15
Quality and efficiency of the implementation	40	15
Total	100	60

Relevance	5	3
Relevance	5	3
Implementation	5	3
Impact	5	3
Total	15	10

A proposal needs to have **passed the thresholds in both** evaluations to be selected as the Hosting Consortium and to be awarded the grants.

Chips-2024-CDP-1 : Timetable

Selection of Hosting Consortium milestones	Date and time or indicative period
Call Document Publication	
Publication of this Call Document	25-07-2024
Submission of applications	
Calls Deadline	10-10-2024 - 17:00
Application Opening day (open of envelopes with expressions of interest)	
Evaluation	November 2024
Selection by Public Authorities Board	December 2024
Notification of results to applicants	
Signature of the hosting agreement	January 2025
Signature of hosting agreement	
Signature of grant agreements	

Further Information

- Chips JU website (<https://www.chips-ju.europa.eu/callsinfo/>) for further information on the calls.
- Calls@chips-ju.europa.eu for specific questions related to call documents.
- IT Helpdesk for questions regarding submission issues:
<https://ec.europa.eu/info/funding-tenders/opportunities/portal/screen/support/helpdesks/contact-form>
- EC online manual:
https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/common/guidance/om_en.pdf
- For questions about research and Horizon Europe, you can contact the Research Enquiry Service via the webform :
https://research-and-innovation.ec.europa.eu/contact-us/research-enquiry-service_en
Video on PIC validation: [Your key to EU grants and tenders: the Participant Identification Code \(PIC\) \(youtube.com\)](https://www.youtube.com/watch?v=...)



Thank you for your attention!

