



Submission Guidelines

Call for Pilot Line on Advanced Photonic Integrated Circuits

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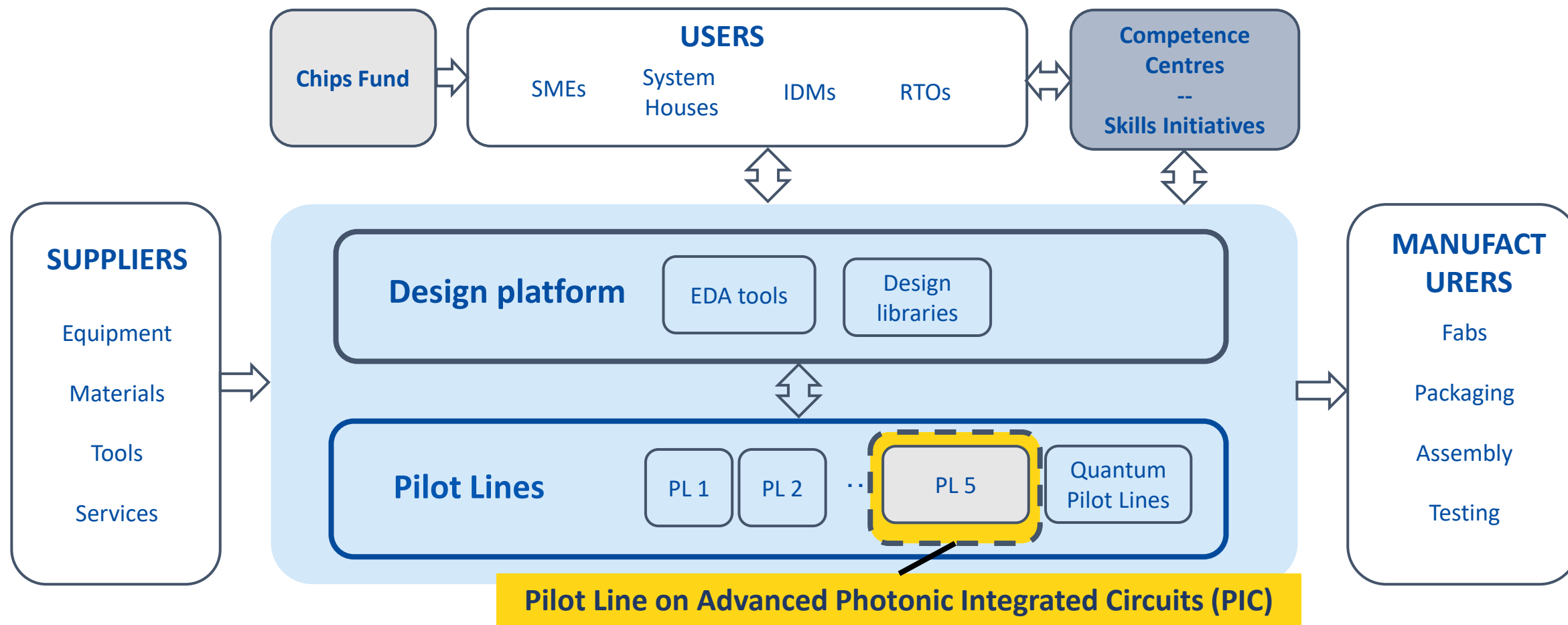
11/07/2024

EUROPEAN
PARTNERSHIP



Chips for Europe Initiative

From lab to fab



PL-5 Call Publication

Chips-2024-CPL-5: Pilot Line on Advanced Photonic Integrated Circuits

EU Expenditure
Max. 180 €Mio

Chips for Europe Initiative Calls

Addressing key objectives such as boosting technological sovereignty, ensuring supply chain resilience, & positioning Europe as a leader in advanced semiconductor technologies.

Open Competence Centres Chips-2024-CCC-1 Click here →	Open Support to the European Network of Chips Competence Centres Chips-2024-CCC-2 Click here →	Coming Soon Pilot Line on Advanced Photonic Integrated Circuits Chips 2023-CPL-5 Click here →	Coming Soon Design platform Chips-2024-CDP-1 Click here →
Closed Pilot line on Advanced sub 2nm leading-edge system on chip technology Chips 2023-CPL-1 Click here →	Closed Pilot line on Advanced Fully Depleted Silicon On Insulator technologies targeting 7nm Chips 2023-CPL-2 Click here →	Closed Pilot line on Advanced Packaging and Heterogenous Integration Chips 2023-CPL-3 Click here →	Closed Pilot line on Advanced semiconductor devices based on Wide Bandgap materials Chips 2023-CPL-4 Click here →

<https://www.chips-ju.europa.eu/callsinfo/>

Publication Date: 4 July 2024

Call Opens: 25 July 2024

**Call Closes: 17 September 2024
(17:00:00 GMT+1)**

Chips-2024-CPL-5: Three Interrelated Calls

Indicative 100 €Mio
Max 150 €Mio
(max 50% EU funding)

Call for Expression of Interest (CfEol)
for the selection of a
Hosting Consortium

Indicative 60 €Mio
Max 100 €Mio
(max 100% EU funding)

**Call for proposals for
Set-up, integration and
process development,**
funded under Horizon
Europe (HE)

Indicative 20 €Mio
Max 40 €Mio
(max 50% EU funding)

**Call for proposals for
the operational
activities of the pilot
line, funded under the
Digital Europe (DEP)**

- Detailed information on <https://www.chips-ju.europa.eu/CPL5/> :

Appendix 4 of the Work
Programme – Activities launched
in 2024 for the initiative part



MAWP Appendix 4
Click here →




Call Documents
Click here →

Call documents: templates and
guidelines – organized in CfEol,
HE and DEP folders

Chips-2024-CPL-5: Context

- Europe's technological **sovereignty and competitiveness** in global markets increasingly hinge on its ability to innovate and maintain leadership in the emerging sector of photonic technologies.
- Pressing need to establish a **dedicated pilot line for PIC within Europe** (particularly extending operational wavelengths from the near-infrared into the visible and mid-infrared spectrums).
- New **application areas such as biomedical imaging, quantum computing, and environmental sensing**, which require specific wavelengths for optimal performance.
- Europe needs **critical infrastructure for bridging the gap between laboratory research and industrial-scale production**, towards reliable, scalable, and cost-effective PIC solutions.
- **Foster collaboration among research institutions, SMEs, and large corporations** across Europe, driving innovation, and accelerating the commercialization of PIC technologies.



Chips-2024-CPL-5: Expected Outcomes

- **Develop and enhance PIC technologies** by extending the operational wavelengths into the visible and mid-infrared spectrum.
 - Creation of **intellectual property**.
- **Develop scalable and cost-effective manufacturing processes** for PICs, ensuring compatibility with current industrial standards and promoting widespread adoption.
- **Foster the integration of PICs** with electronic integrated circuits, enhancing the functionality and efficiency of combined systems.
- **Innovate** in the fields of photonic **testing and packaging** to improve reliability, scalability and performance
 - Extend capabilities of PIC technologies to **larger wafer sizes** and **integrate built-in self-test methodologies**
- **Enable rapid prototyping** through Multi-Project Wafer runs, allowing for timely validation and iteration of PIC designs.
- **Develop demonstrators** to validate the advanced PICs technology and to quantify its performance.
- **Develop comprehensive training programs** and skill development initiatives.

Chips-2024-CPL-5: Scope

- **Enhance performance in existing systems**, improving light source technology, detector efficiency, and modulator capabilities, particularly extending into the visible and mid-infrared spectrums.
- **Refinement of the fabrication processes** (optimization of lithography, etching, and deposition processes that allow for the scaling down and increased yield of photonic features).
- **Multi-Project Wafer** runs will be instrumental in the prototyping phase, offering a cost-effective route for validating and iterating PIC designs.
- **Open access** to various PIC technology platforms (especially focusing on SMEs and start-ups), including III-V, Si, SiNx and hybrid-integration.
- Continuously deliver updated **Process Design Kits (PDKs)** and **Assembly Design Kits (ADKs)** that reflect the advancements in PIC technologies.
- **Promote the collaboration** with other pilot lines, with design platforms and competence centres.

Chips-2024-CPL-5: Focus of the Calls

Chips-2024-CPL-5: Pilot Line on Advanced Photonic Integrated Circuits

Call for Expression of Interest (CfEol)

- Hosting Consortium
- Procurement management including facilities and equipment (existing and to be built)
-

Call for proposals for Set-up, integration and process development (HE)

- Equipment commissioned (materials, technology modules, metrology)
- Process flows set up (recipes, methods)
- Demonstrators
-

Call for proposals for the operational activities of the pilot line (DEP)

- Offered technologies/capacity
- Business model
- Access and services to the wider community
- Skills development and access to training
-

Chips-2024-CPL-5: Hosting Consortium

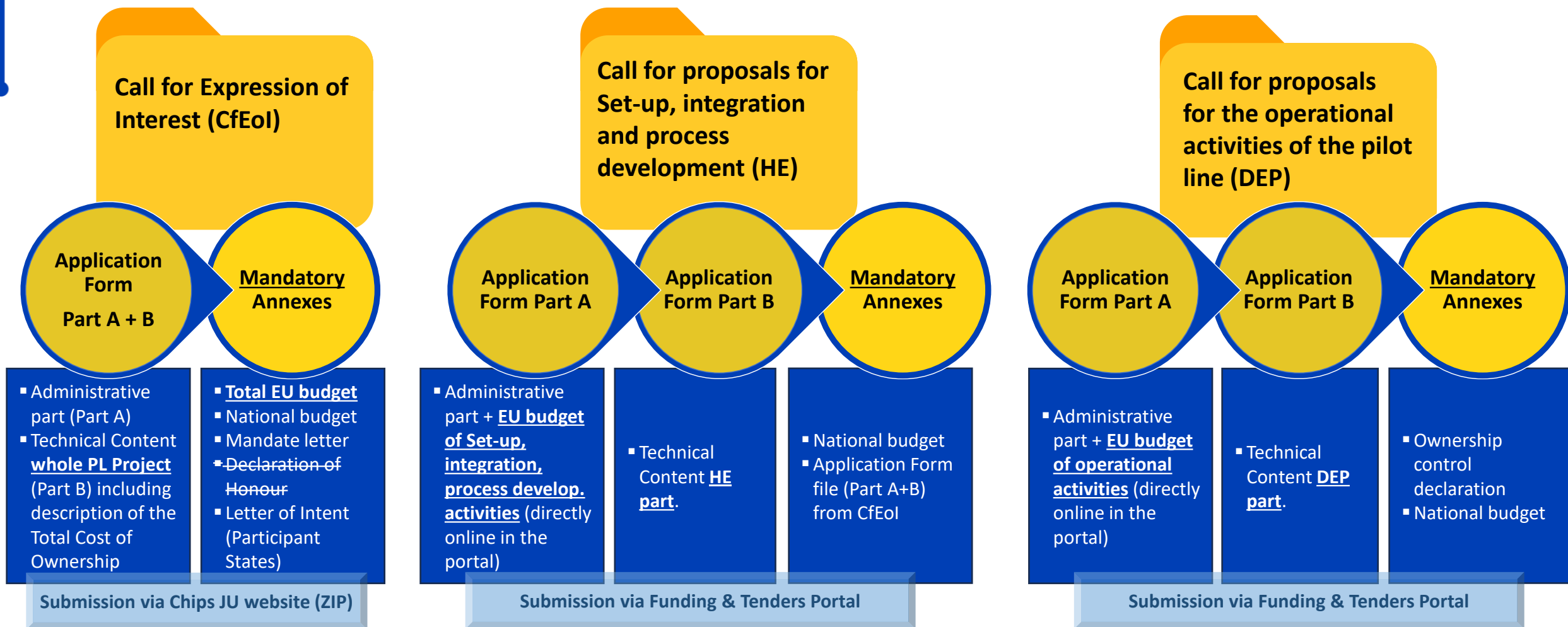
- A consortium needs to include:
 - a) **at least one** independent legal entity established **in a Member State**; and
 - b) at least **two other** independent legal entities each established **in different Participating States***.
- The consortium ('Hosting Consortium'), will be composed of **one or more Hosting Entities** (i.e., entities that are hosting part or all of the equipment and tools of the pilot line) and possibly other members.
- One of the consortium members acts as the **coordinator**; typically, but not necessarily, the coordinator is a Hosting Entity.

*Entities established in Participating States that are associated countries (i.e., not in a Member State) will only receive funding from the Programme (HE and/or DEP) their countries are associated to.

Chips-2024-CPL-5: Access Guiding Principles

- Access needs to be open to a wide range of public and private users across the Union and granted on a **transparent and non-discriminatory** basis directly proportional to the financial contribution by the Union to the total costs of those activities.
- Access needs to be provided on **market terms**, or on a cost-plus-reasonable-margin basis for large undertakings, while granting **preferential access or reduced prices** for **academic institutions, start-ups and SMEs**.
- **PDKs/ADKs** need to be accessible for different categories of users (academia, research, industry etc.) and will be **required to be available via the European Design Platform**.
- Access conditions for non-EU organisations need to take into account the Union's commitments to **international cooperation under its strategic partnerships**.

Chips-2024-CPL-5: Submission Documents



Chips-2024-CPL-5: Technical Content

- **Application Form** of CfEol contains the **whole technical proposal in a single file**.
- **Highly recommended:** please keep the whole proposal consistent and comprehensible.
 - E.g.: structured and articulated organization of concepts, equipment, processes, services up to access and business plans.

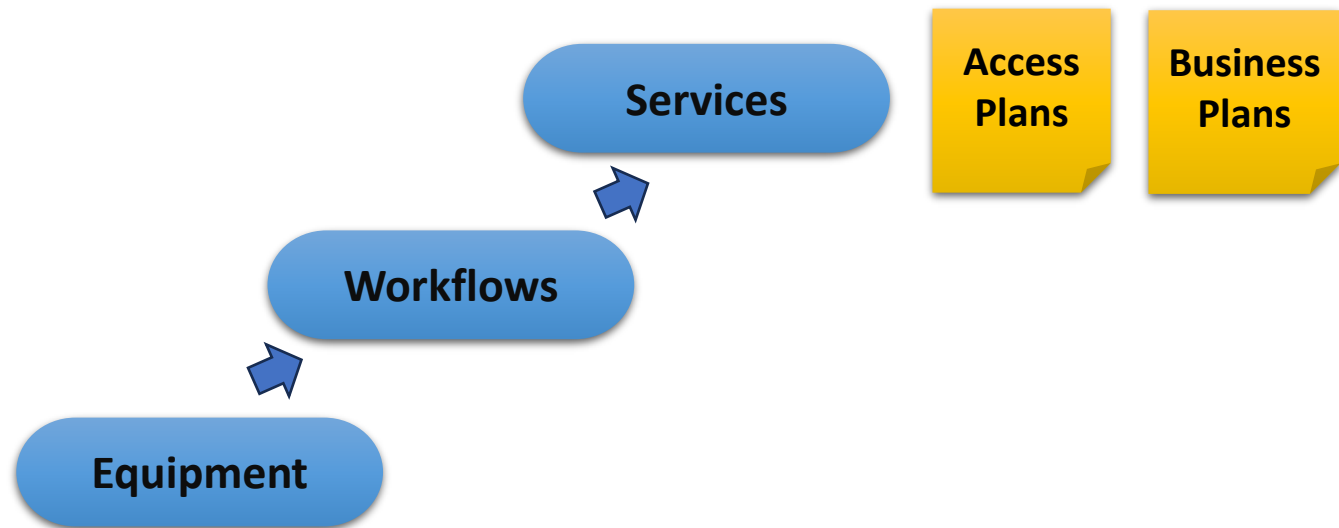
Application Form Template

PART A

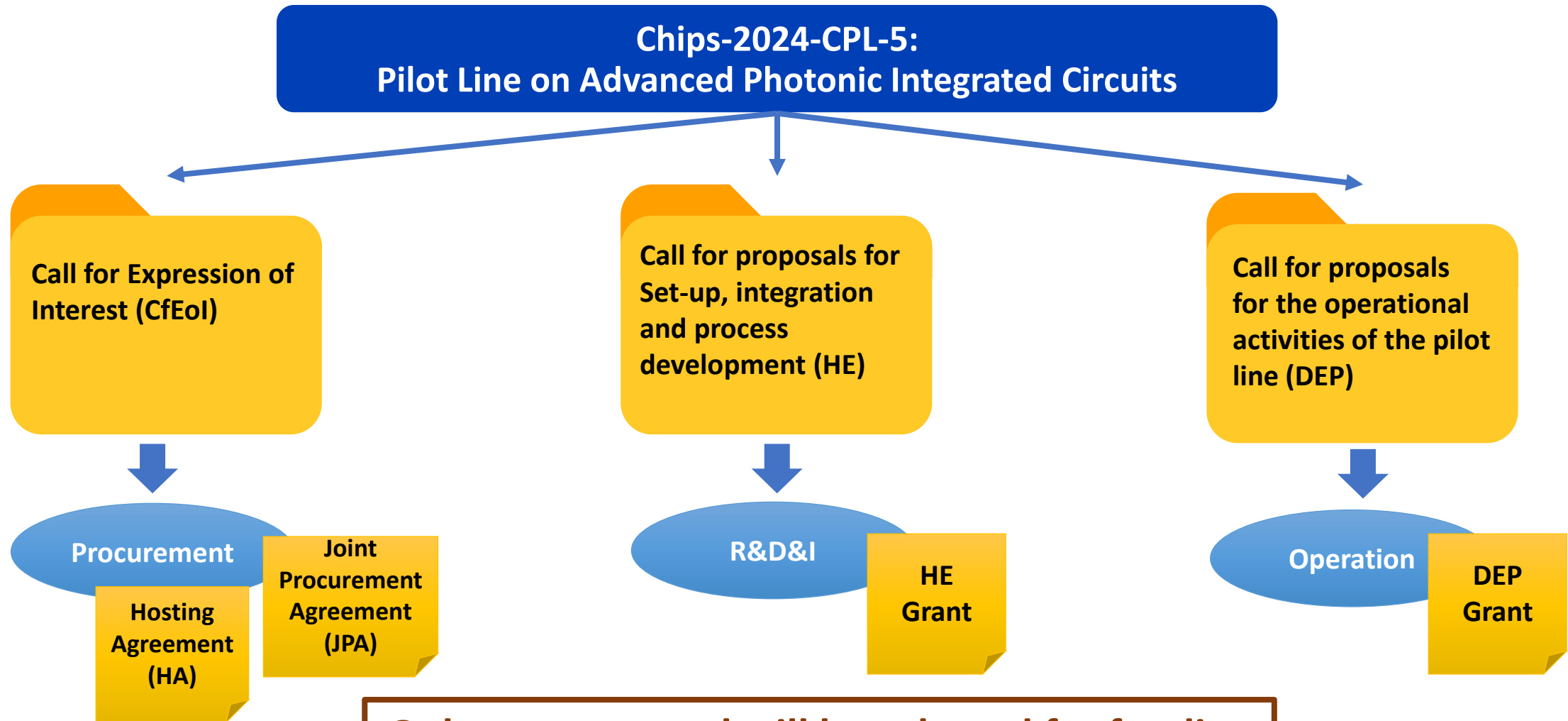
PART B

1. Excellence and Relevance
 - 1.1 Objectives and ambition
 - 1.2 Methodology
2. Impact
 - 2.1 Pathways towards impact
 - 2.2 Measures to maximize impact
3. Quality and efficiency of the implementation
 - 3.1 Maturity
 - 3.2 Implementation plan and efficient use of resources
 - 3.3 Capacity to carry out the proposed work
 - 3.4 Work plan and resources

DESCRIPTION OF THE TOTAL COST OF OWNERSHIP



Chips-2024-CPL-5: Outcomes of the Calls



Only one proposal will be selected for funding

Chips-2024-CPL-5: Evaluation

Chips-2024-CPL-5: Pilot Line on Advanced Photonic Integrated Circuits

Call for Expression of Interest (CfEol)

Criterion	Max Score	Threshold
Excellence & Relevance	30	15
Impact	30	15
Quality and efficiency of the implementation including the Total Cost of Ownership	40	15
Total	100	60

Call for proposals for Set-up, integration and process development (HE)

Criterion	Max Score	Threshold
Relevance	5	3
Implementation	5	3
Impact	5	3
Total	15	10

Call for proposals for the operational activities of the pilot line (DEP)

Relevance	5	3
Relevance	5	3
Implementation	5	3
Impact	5	3
Total	15	10

*It will be Normalized for Evaluation purposes.

A proposal needs to have **passed the thresholds in the three** evaluations to be selected

Chips-2024-CPL-5: Timetable

Selection of Hosting Consortium milestones	Date and time or indicative period
Call Document Publication	
Publication of this Call Document	25-07-2024
Submission of applications	
Calls Deadline	17-09-2024 - 17:00
Application Opening day (open of envelopes with expressions of interest)	
Evaluation	October 2024
Selection by Public Authorities Board	November 2024
Notification of results to applicants	
Signature of the hosting agreement	December 2024
Signature of hosting agreement	May 2025
Signature of grant agreements	

Further Information

- Chips JU website (<https://www.chips-ju.europa.eu/callsinfo/>) for further information on the calls.
- Calls@chips-ju.europa.eu for specific questions related to call documents.
- IT Helpdesk for questions regarding submission issues:
<https://ec.europa.eu/info/funding-tenders/opportunities/portal/screen/support/helpdesks/contact-form>
- EC online manual:
https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/common/guidance/om_en.pdf
- For questions about research and Horizon Europe, you can contact the Research Enquiry Service via the webform :
https://research-and-innovation.ec.europa.eu/contact-us/research-enquiry-service_en
Video on PIC validation: [Your key to EU grants and tenders: the Participant Identification Code \(PIC\) \(youtube.com\)](https://www.youtube.com/watch?v=...)



Thank you for your attention!





EU added value and economic security considerations

- Access to pilot lines should be based on **fair and non-discriminatory principles** and should be **limited to Participating States of the Chips JU** (EU Member States, EEA countries and those countries that have been associated to Horizon Europe or Digital Europe Strategic Objective 6, under which the design platform is funded).
- For access of users **established in any Participating State** but **controlled from third countries** that are not Participating States of the Chips JU, consortia must take into consideration the following two main criteria:
 - **EU added value**, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.
 - **Economic security** considerations.

Only users from organisations that can clearly **demonstrate** their **contribution to EU added value** and their alignment with **European economic security** shall be granted access.